Au-NiW Mechanically Flexible Interconnects (MFIs) and TSV Integration for 3D Interconnects

Chaoqi Zhang, Paragkumar Thadesar, Muneeb Zia, Thomas Sarvey, and Muhannad S. Bakir
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, Georgia, 30332
Email: chqzhang@gatech.edu ; muhannad.bakir@mirc.gatech.edu

***Abstract*—Mechanically Flexible Interconnects (MFIs) with a pitch of 50 µm and a standoff height of 65 µm are reported. Mechanical characterization of the MFIs using indentation demonstrates elastic deformation and the feasibility of temporary interconnection. The integration of MFIs and TSVs is also reported along with electrical testing for interposer and 3D IC applications.**

Keywords—Flexible interconnect; TSV; 3D integration

I. Introduction

High bandwidth density and low energy-per-bit off-chip interconnects are critical to enable substantial system throughput improvement in modern computing systems [1-3]. As shown in Figure 1, there is significant interest in placing a memory stack and a CPU die side-by-side on an interposer [4-5]. Such chips would be permanently soldered onto the interposer, which provides high-bandwidth routing. However, such a 3D integration platform suffers from the inability to perform system level testing with repair capability, which may be critical to lowering system cost by improving yield in some applications. Therefore, we propose a rematable 3D integration platform using Au-NiW based mechanically flexible interconnects (MFIs). As shown in Figure 1, the solder interconnections, which consist of C4 bumps (between the interposer and the organic substrate) and micro-bumps (between the dice and the interposer), may be replaced by the flexible I/Os under consideration. Using the Au-NiW MFIs, the system can be repaired by replacing components as necessary.

Limited by either their range of motion or pitch scalability, it is challenging for previously investigated flexible I/O technologies [6-8] to be used in the proposed 3D integration platform. Based on the Au-NiW MFIs previously developed by our group [9-11], in this paper, we report Au-NiW MFIs with high range of motion, highly scalable pitch, and large contact force to enable a rematable interconnect for 3D integration.

The paper is organized as follows: the MFI fabrication process and mechanical tests are discussed in Section II. In Section III, preliminary MFI and TSV integration is conducted to demonstrate the process compatibility. Electrical DC resistance measurements are performed as well.

II. Mechanically Flexible Interconnects

In this section, we report the wafer-level batch fabrication process to form MFI-arrays with various pitch values. MFI mechanical indentation tests are reported as well to demonstrate their flexibility.

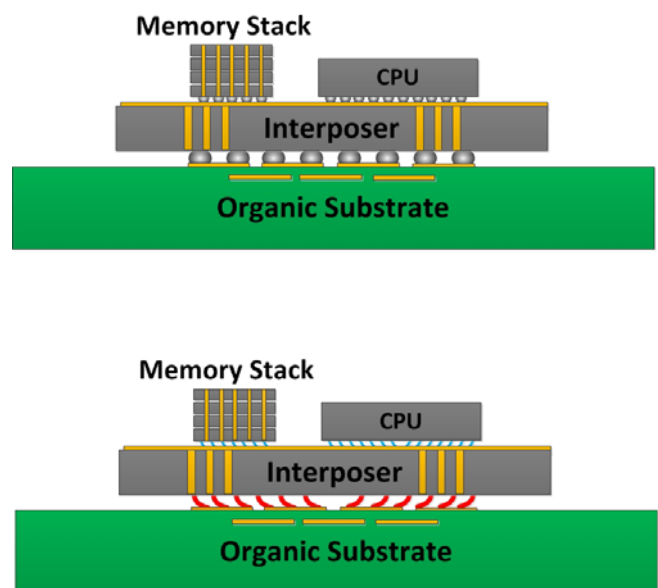

Figure 1 Conventional 3D integration using solder joints (top) and rematable 3D integration enabled by Au-NiW MFIs (bottom)

A. MFI Fabrication Process Based on Photoresist Spray-coating

The wafer-level batch fabrication process of the MFIs under consideration in this paper is illustrated in Figure 2. First, a spin-coated polymer layer is patterned and thermally reflowed to form sacrificial domes on a nitride passivated silicon wafer. Next, a Ti/Cu/Ti film is sputtered on top of the domes and used as the electroplating seed layer. A conformal photoresist layer is, next, formed above the seed layer using spray-coating and subsequently patterned to form the MFI electroplating (NiW) mold. Once the MFIs are electroplated, the seed layer and the sacrificial domes are stripped leaving behind MFIs on the substrate. To avoid oxidization of the NiW film, an immersion gold process is used to enhance the reliability and extend the lifetime.

As shown in step E of Figure 2, a conformal electroplating mold is critical in obtaining a fine pitch MFI array while

978-1-4799-8472-5/14/$31.00 ©2014 IEEE

maintaining a large standoff height. As reported in [9], the MFI electroplating mold was previously formed using photoresist spin-coating. Unfortunately, that process resulted in a thin resist film at the peak of the domes and a thick resist film in the valley between the domes (Figure 3). The non-uniform photoresist thickness induces severe undercut of the electroplating mold during photolithography and results in shorts between adjacent MFIs after electroplating. Therefore, photoresist spin-coating is not a feasible process to form fine pitch MFIs with a large vertical gap. By using photoresist spray-coating, a conformal photoresist layer with uniform thickness, as shown in Figure 4, can be obtained. This photoresist uniformity enables 'perfect' exposure of the photoresist across the substrate (Figure 5).

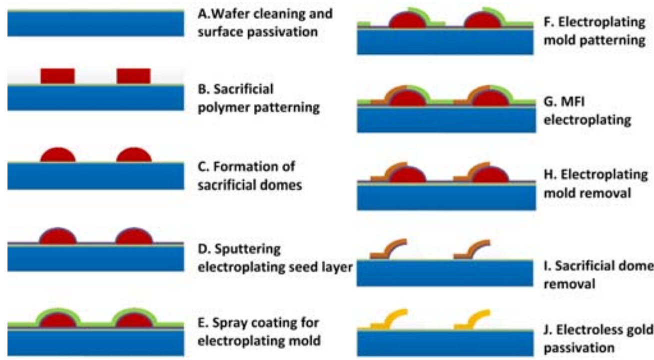

Figure 2 Fabrication process of the NiW MFIs with gold passivation layer using photoresist spray coating

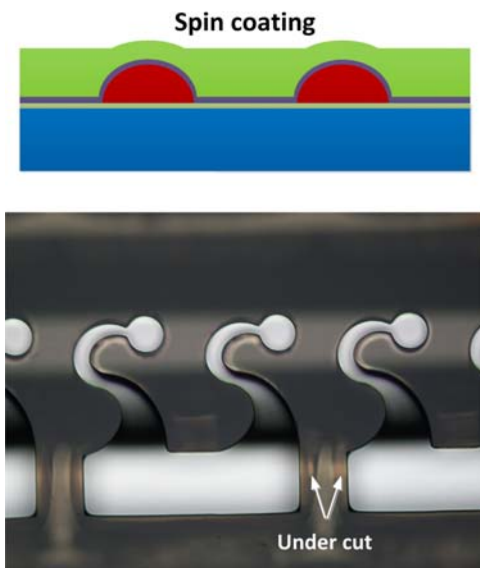

Figure 3 Fabrication challenges associated with MFI processing using photoresist spin-coating (for the electroplating mold layer)

Figure 6 illustrates free-standing Au-NiW MFIs with a standoff height of 65 µm and a pitch of 150 µm. Moreover, the pitch can be scaled to 50 µm while maintaining the 65 µm standoff height, as shown in Figure 7. Note that the MFI footprint is reduced as the pitch decreases.

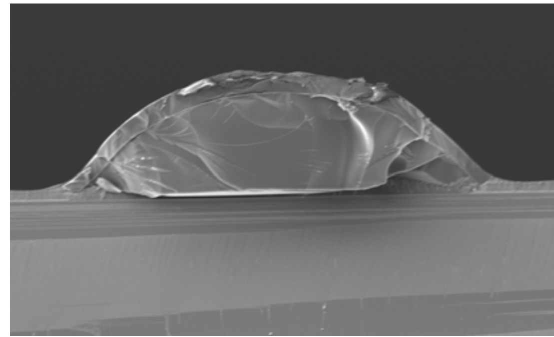

Figure 4 Photoresist spray-coating was used to form a conformal electroplating mold on top of sacrificial polymer domes.

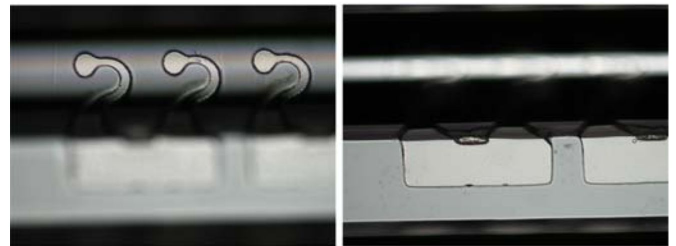

Figure 5 MFIs on polymer domes after removing electroplating mold

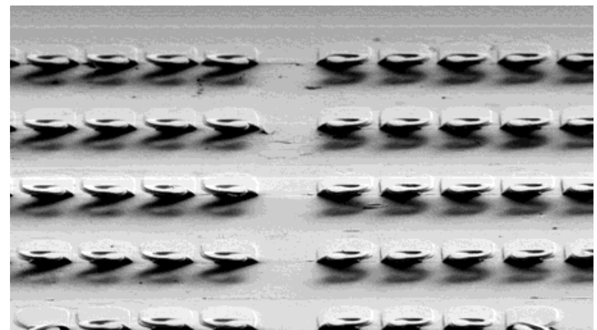

Figure 6 Au-NiW MFIs on 150 µm pitch

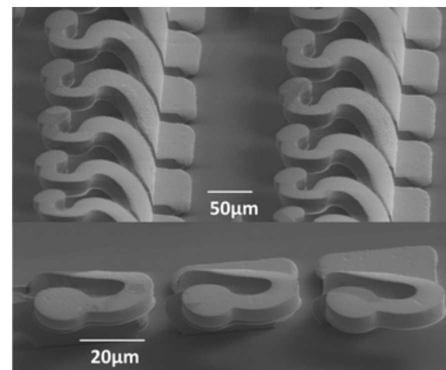

Figure 7 Au-NiW MFIs on 50 µm pitch

B. Mechanical Characterization

Figure 8 MFI indentation test performed using a piezo-driven indentation head

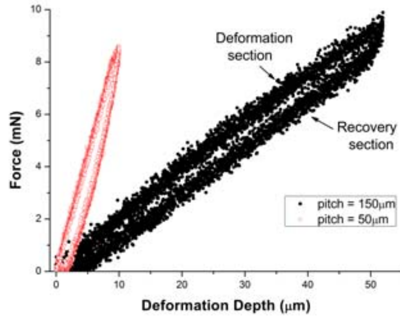

Figure 9 Indentation tests of MFI on a pitch of 150 μm and 50 μm

In order to evaluate the mechanical properties of the MFI, indentation tests are performed using a Hysitron Triboindenter. As shown in Figure 8, each indentation cycle includes a deformation and a recovery period. During the deformation period, the MFI is deformed downward to a predefined depth using a piezo-driven indentation head; during the recovery period, the MFI is released to recover its pre-deformation profile. The real-time position and corresponding reaction force are plotted in Figure 9. For MFIs on the 50 μm pitch, the measured bending force is 8.4 mN for 10 μm deformation, which results in a compliance of 1.20 mm/N; for MFIs on 150 μm pitch, the measured bending force is 9.4 mN for 50 μm deformation, which results in a compliance of 5.32 mm/N. When the indentation head is completely released from the MFI (force is 0 mN), the MFI recovers its pre-deformation position (deformation depth is 0 μm). Because of the full recovery, the MFIs demonstrate elastic deformation and a promising interconnect technology for rematable assembly.

III. MFIs FOR 3D INTEGRATION

In this section, the process integration of MFIs and TSVs is reported.

A. Fabrication Process

As shown in Figure 10, the TSVs in this work were fabricated using the 'mesh process' developed previously [12]. The fabrication process of MFI/TSV integration begins with silicon via etching using STS ICP from the top side of the wafer and mesh etching using Vision RIE from the back side of the wafer. After silicon oxide liner deposition, the mesh side of the wafer is pinched-off and the via is filled by Cu electroplating followed by chemical mechanical polishing (CMP) to remove the over-electroplated Cu. The TSV process ends with back side routing layer formation. Next, the MFI process is performed on the wafer with TSVs using processes similar to those discussed in section II. The dimensions of the fabricated MFI/TSV array are summarized in Table 1.

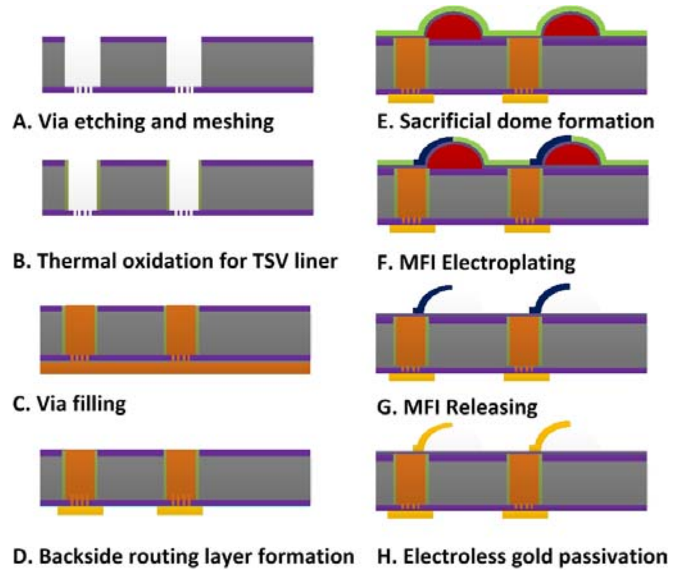

Figure 10 Fabrication process of MFI/TSV integration

TABLE 1 DIMENSIONS OF MFI/TSV ARRAY

TSV	Diameter (μm)	50
	Height (μm)	300
	Pitch (μm)	100
MFI	Vertical height (μm)	30
	Thickness (μm)	5
	Pitch (μm)	100

X-ray images of the fabricated sample are shown in Figure 11. The top image in the figure shows the good alignment of the MFIs and the TSVs. The second (bottom) image in the figure shows the fully filled Cu vias without voids as well as good interconnection at the TSV-MFI interface (based on visual inspection).

B. *Assembly and Electrical Characterization*

As shown in Figure 12, using a flip-chip bonder, a silicon chip with MFIs and TSVs is assembled on a silicon substrate with a gold-coated surface (with silicon dioxide in-between). Using this setup, four-point resistance measurements are performed to measure the resistance of each MFI/TSV pair plus the contact resistance between the MFI and the gold surface. The measured resistance is 76 mΩ, which agrees well with calculated values.

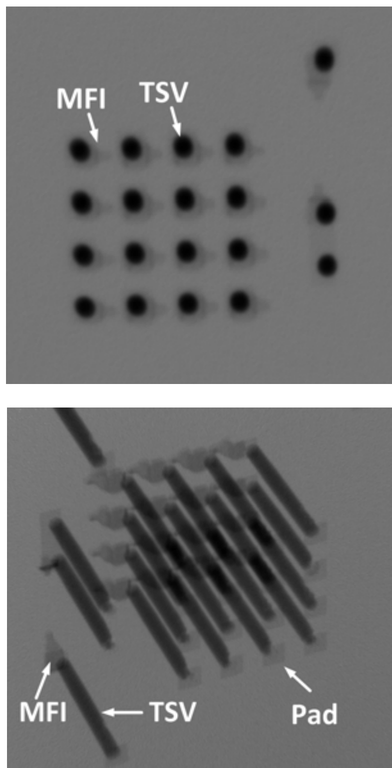

Figure 11 X-ray image of TSV/MFI integration: top view (top) and angled view (bottom)

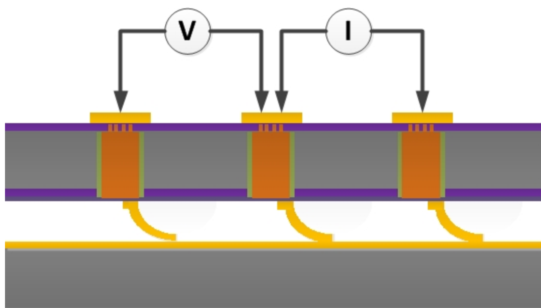

Figure 12 TSV/MFI four-point electrical resistance measurement setup

IV. Conclusion

A wafer-level batch fabricated mechanically flexible interconnect technology using gold-coated NiW has been developed for interposer and 3D IC integration applications. A CMOS compatible fabrication process using photoresist spray-coating enables the formation of MFI arrays with a large range of pitch values (150 µm to 50 µm) while maintaining 65 µm standoff height. The rematable 3D integration capability of the Au-NiW MFIs is verified using the following: 1) indentation test results indicate that the Au-NiW MFIs can fully recover their pre-deformation profile; 2) MFI/TSV process integration illustrates the feasibility of using MFIs in a 3D IC process flow; 3) four-point electrical resistance measurements using assembled chips with MFIs and TSVs meet predicted values thereby demonstrating process fidelity.

Acknowledgment

The authors would like to thank David Hopkins and Michael Dayringer at Oracle Labs, and Hiren Thacker, John Cunningham, Ivan Shubin, and Kannan Raj at Oracle for valuable discussions and support.

References

[1] B. Banijamali et al., "Assembly and Reliability Challenges in 3D Integration of 28nm FPGA Die on a Large High Density 65nm Passive Interposer," in Proc. Electronic Components and Technology Conference, pp. 279-283, 2012.

[2] I. Shubin et al., "Scaling Hybrid-Integration of Silicon Photonics in Freescale 130nm to TSMC 40nm-CMOS VLSI Drivers for Low Power Communications" , in Proc. Electronic Components and Technology Conference, pp. 1518-1525, 2012.

[3] M. Vinet, P. Batude, C. Tabone, B. Previtali, C. LeRoyer, A. Pouydebasque, L. Clavelier, A. Valentian, O. Thomas, S. Michaud, L. Sanchez, L. Baud, A. Roman, V. Carron, F. Nemouchi, V. Mazzocchi, H. Grampeix, A. Amara, S. Deleonibus, O. Faynot, "3D monolithic integration: Technological challenges and electrical results", Microelectronic Engineering, Vol. 88, pp. 331-335, 2011.

[4] http://www.eetimes.com/author.asp?section_id=36&doc_id=1285974

[5] http://www.extremetech.com/computing/167368-hybrid-memory-cube-160gbsec-ram-starts-shipping-is-this-the-technology-that-finally-kills-ddr-ram

[6] I. Shubin, E. Chow, J. Cunningham, D. De Bruyker, C. Chua, B. Cheng, J. C.Knights, K. Sahasrabuddhe, Y. Luo, A. Chow, J. Simons, A. Krishnamoorthy,R. Hopkins, R. Drost, R. Ho, D. Douglas, and J. Mitchell, "Novel packaging with rematable spring interconnect chips for mcm," in Proc. Electronic Components and Technology Conference, pp. 1053–1058, 2009.

[7] Q. Zhu, L. Ma, and S. Sitaraman, "Design optimization of one-turn helix: a novel compliant off-chip interconnect," IEEE Trans. Advanced Packaging, vol. 26, no. 2, pp. 106–112, 2003.

[8] S. Muthukumar, C. Hill, S. Ford, W. Worwag, T. Dambrauskas, P. Challela, T. Dory, N. Patel, E. Ramsay, and D. Chau, "High-density compliant die-package interconnects," in Proc. Electronic Components and Technology Conference, pp. 1233-1238, 2006.

[9] C. Zhang, H. S. Yang and M. Bakir, "Highly elastic gold passivated mechanically flexible interconnects," IEEE Trans. Components, Packaging and Manufacturing Technology, vol. 3, pp. 1632-1639, 2013.

[10] C. Zhang, H. S. Yang and M. Bakir, "Mechanically flexible interconnects (MFIs) with highly scalable pitch," Journal of Micromechanics and Microengineering, Vol. 24, no. 5, pp. 055024-1-055024-8, 2014.

[11] C. Zhang, H.S. Yang, M. Bakir, "Mechanically Flexible Interconnects with Highly Scalable Pitch and Large Stand-off Height for Silicon Interposer Tile and Bridge Interconnection," in Proc. Electronic Components and Technology Conference, pp. 13-19, 2014.

[12] J.-H Lai, H. S. Yang, H. Chen, C. King, J. Zaveri, R. Ravindran, and M. Bakir, "A 'mesh' seed layer for improved through-silicon-via fabrication," Journal of Micromechanics and Microengineering, vol. 20., pp. 025016, 2010.